

# STRUCTURES AND METHODS FOR IMPROVED CAPACITOR CELLS IN INTEGRATED CIRCUITS

## Related Applications

This application is a Divisional of U.S. Serial Number 09/499,726, filed on February 8, 2000, the specification of which is incorporated herein by reference.

This application is related to the following co-pending and commonly  
5 assigned application: U. S. Serial Number 09/364852 filed July 30, 1999, (attorney  
docket number 303.609US1) now issued as U.S. Patent No. 6,465,828 on October  
15, 2002, entitled Semiconductor Container Structure with Diffusion Barrier, which  
is hereby incorporated by reference.

## Technical Field

10 The technical field relates generally to semiconductor integrated circuits.  
More particularly, it pertains to capacitors in semiconductor integrated circuits.

## Background

15 A capacitor is composed of two layers of a material that is electrically  
conductive (hereinafter, electrode) brought near to one another and separated by a  
material that is electrically nonconductive. Suppose the capacitor is connected to a  
battery with a certain voltage level (hereinafter, energy level). Charges will flow  
from the battery to be stored in the capacitor until the capacitor exhibits the energy  
20 level of the battery. Then, suppose further that the capacitor is disconnected from  
the battery. The capacitor will indefinitely exhibit the energy level of the battery  
until the charges stored in the capacitor are removed either by design or by accident.

This ability of the capacitor to “remember” an energy level is valuable to the  
operation of semiconductor integrated circuits. Often, the operation of such circuits  
25 may require that data be stored and retrieved as desired. Because of its ability to

remember, the capacitor is a major component of a semiconductor memory cell. One memory cell may store one bit of data. A system of memory cells is a semiconductor memory array where information can be randomly stored or retrieved from each memory cell. Such a system is also known as a random-access memory.

5           One type of random-access memory is dynamic random-access memory (DRAM). The charges stored in DRAM tend to leak away over a short time. It is thus necessary to periodically refresh the charges stored in the DRAM by the use of additional circuitry. Even with the refresh burden, DRAM is a popular type of memory because it can occupy a very small space on a semiconductor surface. This  
10 is desirable because of the need to maximize storage capacity on the limited surface area of an integrated circuit.

          One type of capacitor that supports an increase in storage capacity uses an electrode composed of a metal compound. So that charges can be transferred into and out of the capacitor, a metallization layer is placed in connection with the metal  
15 compound electrode of the capacitor. The metallization layer may act with the metal compound to create a region that is electrically nonconductive. That act compromises the ability of charges to move into and out of the capacitor at the junction of the electrode. This effect is detrimental to the storage ability of a capacitor and would render a memory cell defective. One solution that has been  
20 proposed is to use polysilicon as a layer in contact with the capacitor. However, this solution is inadequate in that the polysilicon may act at a certain temperature with the metal compound electrode of the capacitor to form an electrically nonconductive region.

          Thus, what is needed are systems, devices, structures, and methods to inhibit  
25 the described effect so as to maintain electrical contact between the metallization layer and the capacitor.

### Summary

The above-mentioned problems with capacitors as well as other problems are addressed by the present invention and will be understood by reading and studying  
5 the following specification. Systems, devices, structures, and methods are described which accord these benefits.

An illustrative embodiment includes a capacitor. The capacitor comprises a first electrode, a first dielectric coupled to the first electrode, and a second electrode coupled to the first dielectric. The second electrode includes an inhibiting layer so  
10 as to inhibit formation of an undesired second dielectric.

Another illustrative embodiment includes a capacitor. The capacitor comprises a first electrode that comprises at least one conductive metal oxide. The conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide. The capacitor includes a dielectric coupled to the first electrode. The  
15 dielectric comprises at least one insulator metal oxide. The metal oxide includes ditantalum pentaoxide. The capacitor includes a second electrode. The second electrode comprises the conductive metal oxide that is selected from a group consisting of ruthenium oxide and iridium oxide. The second electrode also comprises an inhibiting layer. The inhibiting layer comprises a substance selected  
20 from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy. The transition metal is selected from a group consisting of platinum, rhodium, and tungsten. The transition metal alloy includes a platinum rhodium alloy. The nitride compound is selected from a group consisting of tungsten nitride and titanium nitride. The noble metal includes  
25 platinum, gold, titanium, and silver. The noble metal alloy includes graphite, chlorimet 3, and hastelloy C.

Another illustrative embodiment includes a semiconductor structure. The semiconductor structure includes an insulation layer and a first conductive layer

abutting the insulation layer. The first conductive layer includes an inhibiting layer that inhibits a diffusion that increases resistivity.

Another illustrative embodiment includes a semiconductor structure. The semiconductor structure includes an insulation layer and a first conductive layer abutting the insulation layer. The first conductive layer includes an inhibiting layer that inhibits formation of an undesired oxidation compound so as to enhance an ohmic contact.

Another illustrative embodiment includes a method of forming a semiconductor structure. The method comprises forming a first conductive layer, forming an insulation layer abutting the first conductive layer, forming a second conductive layer abutting the insulation layer, and forming an inhibiting layer abutting the second conductive layer. The inhibiting layer inhibits formation of an undesired oxidation compound so as to enhance an ohmic contact.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

#### Brief Description of the Drawings

Figure 1 is a cross-sectional view of a semiconductor structure according to one embodiment of the present invention.

Figure 2 is an elevation view of a semiconductor memory array according to one embodiment of the present invention.

Figures 3A-3O are cross-sectional views of a semiconductor structure during processing according to one embodiment of the present invention.

Figure 4 is a block diagram of a device according to one embodiment of the present invention.

5        Figure 5 is an elevation view of a semiconductor wafer according to one embodiment of the present invention.

Figure 6 is a block diagram of a circuit module according to one embodiment of the present invention.

10       Figure 7 is a block diagram of a memory module according to one embodiment of the present invention.

Figure 8 is a block diagram of a system according to one embodiment of the present invention.

Figure 9 is a block diagram of a system according to one embodiment of the present invention.

15       Figure 10 is a block diagram of a system according to one embodiment of the present invention.

#### Detailed Description

20       In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized  
25       and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

The terms wafer and substrate used in the following description include any base semiconductor structure. Both are to be understood as including

silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor structure, as well as other semiconductor structures well known to one skilled in the art. Furthermore, when  
5 reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure and layer formed above, and the terms wafer or substrate include the underlying layers containing such regions/junctions and layer that may have been formed above. The following detailed description is, therefore, not to be  
10 taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

Figure 1 is a cross-sectional view of a semiconductor structure according to one embodiment of the present invention. The semiconductor structure 100 may illustrate an example of a single DRAM cell. The semiconductor structure 100 includes a  
15 substrate 102, field isolators 104, transistor 134, insulation layers 120 and 122, another semiconductor structure such as a capacitor 136, and a metallization layer 140. The transistor 134 includes source/drain regions 106<sub>0</sub> and 106<sub>1</sub>, silicide region 108, spacers 112, gate oxide 114, and gate 116. The source/drain regions 106<sub>0</sub> and 106<sub>1</sub> include lightly doped source/drain regions 110. The capacitor 136 includes an electrode 124, a  
20 dielectric layer 126, another electrode 128, and an inhibiting layer 130. The dielectric layer 126 is coupled to the electrodes 124 and 128. The term “metallization layer” means the inclusion of a layer where various regions of each circuit element are in contact and proper interconnection of the circuit element is made. The term  
“metallization layer” means the inclusion of a diffusion barrier or refractory silicides.  
25 The term “metallization layer” means the inclusion of wiring to interconnect various devices in an integrated circuit.

Charges can be transferred into or removed from the capacitor 136 by turning on the transistor 134. The transistor 134 is turned on by an appropriate voltage level and

polarity placed at the gate 116 so that a depletion region and conducting channel are formed between the source/drain regions 106<sub>0</sub> and 106<sub>1</sub>. If charges are to be transferred into the capacitor 136, these charges are introduced at the source/drain region 106<sub>0</sub> by a buried bit line 141, so that they may travel across the conducting channel into the source/drain region 106<sub>1</sub>, conduct through the metallization layer 140, conduct through the inhibiting layer 130, and enter the electrode 128. The charges cannot go any further because the dielectric layer 126 is electrically nonconductive. However, these charges will attract opposite polarity charges to appear at electrode 124. Hence, an electric field is set up between the electrodes 128 and 124. Energy is stored in this electric field.

10 This electric field is the phenomenon that allows the capacitor to “remember.”

There exists an industry-wide drive to smaller memory cells to increase storage density on the limited surface area of an integrated circuit. This has motivated the use of a metal oxide conductive material for use as an electrode of the capacitor 136. Without the inhibiting layer 130, this metal oxide conductive material may undesirably act with the metallization layer 140 when the temperature reaches about 400 degrees Celsius or greater. Such act may form an undesired oxide compound that prevents charges from being able to enter or exit the capacitor 136. Thus, because of the undesired oxide compound, an opened contact exists between the metallization layer 140 and the capacitor 136.

20 The physics of solids may explain this problem. Diffusion is a process that includes materials intermixing on the molecular scale. Although diffusion is readily seen in the mixing of two different liquids, such as ink and water, diffusion also occurs in solids, albeit slowly. One reason why diffusion through solids is slow is because of the tight crystal structures of solids. In such tight crystal structure, molecules that

25 diffuse through a solid would require such a large amount of energy so as to render diffusion nearly impossible. However, at sufficiently high temperature, defects are introduced into the crystal structure such that vacancy in the structure may arise. This

vacancy allows diffusion to occur more easily in solids.

Returning to Figure 1, at temperature of about 400 degrees Celsius, a portion of the metallization layer 140 may have structural defects, such as vacancy. Vacancy allows the oxygen ions in the metal oxide conductive material of the electrode 128 to  
5 diffuse through to the metallization layer 140 to form an insulator oxide compound. In the case where the metallization layer 140 includes a layer of titanium, such diffusion may form a titanium oxide compound, which is an insulator. Such a compound compromises the electrical contact between the metallization layer 140 and the capacitor 136.

10 The inhibiting layer 130 acts to inhibit such compromise from occurring. In one embodiment, the inhibiting layer 130 acts to enhance the conductivity between the metallization layer 140 and the capacitor 136. In another embodiment, the inhibiting layer 130 acts to inhibit formation of an undesired dielectric between the metallization layer 140 and the electrode 128. In another embodiment, the inhibiting layer 130 acts to  
15 inhibit a diffusion that increases resistivity between the metallization layer 140 and the electrode 128. In another embodiment, the inhibiting layer 130 acts to inhibit formation of an undesired oxidation compound so as to enhance an ohmic contact between the metallization layer 140 and the electrode 128. The term "ohmic contact" means the inclusion of a metal-metal contact, metal-semiconductor contact, or semiconductor-semiconductor contact that has an approximately linear current-voltage characteristic. In  
20 another embodiment, the inhibiting layer 130 includes a layer that is disposed on the electrode 128. In another embodiment, the inhibiting layer 130 includes a layer that is embedded in the electrode 128. In one embodiment, the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy. In one embodiment, the  
25 transition metal is selected from a group consisting of platinum, rhodium, and tungsten. In another embodiment, the transition metal alloy includes a platinum rhodium alloy. In



another embodiment, the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride. In a further embodiment, the noble metal includes platinum, gold, titanium, and silver. In yet another embodiment, the noble metal alloy includes graphite, chlorimet 3, and hastelloy C. Although the aforementioned  
5      embodiments focus on the electrode 128, electrode 124 may be used instead if the metallization layer 140 is adapted to contact the electrode 124.

In one embodiment, the electrode 128 comprises at least one conductive metal oxide. In another embodiment, the conductive metal oxide of the electrode 128 is selected from a group consisting of ruthenium oxide and iridium oxide. In another  
10     embodiment, the dielectric 126 comprises at least one insulator metal oxide. In another embodiment, the insulator metal oxide includes ditantalum pentaoxide. In another embodiment, the electrode 124 comprises at least one conductive metal oxide. In yet another embodiment, the conductive metal oxide of the electrode 128 is selected from a group consisting of ruthenium oxide and iridium oxide. In a further embodiment, the  
15     capacitor 136 comprises a combination of the aforementioned embodiments.

Figure 2 is an elevation view of a semiconductor memory array according to one embodiment of the present invention. The memory array 200 includes memory cell regions 242 formed overlying active areas 250. Active areas 250 are separated by field isolation regions 252. Active areas 250 and field isolation regions 252 are formed  
20     overlying a semiconductor substrate.

The memory cell regions 242 are arrayed substantially in rows and columns. Shown in Figure 2 are portions of three rows 201A, 201B and 201C. Separate digit lines (not shown) would be formed overlying each row 201 and coupled to active areas 250 through digit line contact regions 248. Word line regions 244 and 246 are further  
25     coupled to active areas 250, with word line regions 244 coupled to active areas 250 in row 201B and word line regions 246 coupled to active areas 250 in rows 201A and 201C. The word line regions 244 and 246, coupled to memory cells in this alternating

fashion, generally define the columns of the memory array. This folded bit-line architecture is well known in the art for permitting higher densification of memory cell regions 242.

5        Figures 3A-3O are cross-sectional views of a semiconductor structure during processing according to one embodiment of the present invention. Figures 3A-3O are cross-sectional views taken along line A-AN of Figure 2 during various processing stages.

10        Semiconductor structure 300 includes a substrate 302. The substrate 302 may be a silicon substrate, such as a p-type silicon substrate. Field isolators 304 are formed over field isolation regions 352 of the substrate 302. Field isolators 304 are generally formed of an insulator material, such as silicon oxides, silicon nitrides, or silicon oxynitrides. In this embodiment, field isolators 304 are formed of silicon dioxide such as by conventional local oxidation of silicon which creates substantially planar regions of oxide on the substrate surface. Active area 350 is an area not covered by the field  
15        isolators 304 on the substrate 302. The creation of the field isolators 304 is preceded or followed by the formation of a gate dielectric layer 314. In this embodiment, gate dielectric layer 314 is a thermally grown silicon dioxide, but other insulator materials may be used as described herein.

20        The creation of the field isolators 304 and gate dielectric layer 314 is followed by the formation of a conductively doped gate layer 316, silicide layer 308, and gate spacers 312. These layers and spacers are formed by methods well known in the art. The foregoing layers are patterned to form word lines in word line regions 344 and 346. A portion of these word lines is illustratively represented by gates 338<sub>0</sub>, 338<sub>1</sub>, 338<sub>2</sub>, and 338<sub>3</sub>. In one embodiment, the silicide layer 308 includes a refractory metal layer over  
25        the conductively doped gate layer 316, such as a polysilicon layer.

Source/drain regions 306 are formed on the substrate 302 such as by conductive doping of the substrate. Source/drain regions 306 have a conductivity opposite the

substrate 302. For a p-type substrate, source/drain regions 306 would have an n-type conductivity. The source/drain regions 306 include lightly doped source/drain regions 310 that are formed by implanting a low-dose substance, such as an n-type or p-type material. Such lightly doped source/drain regions 310 help to reduce high field in the source/drain junctions of small-geometry semiconductor structure, such as semiconductor structure 300. The portion of the word lines that are illustratively represented by gates 338<sub>0</sub>, 338<sub>1</sub>, 338<sub>2</sub>, and 338<sub>3</sub> is adapted to be coupled to periphery contacts (not shown). The periphery contacts are located at the end of a memory array and are adapted for electrical communication with external circuitry.

The foregoing discussion is illustrative of one example of a portion of a fabrication process to be used in conjunction with the various embodiments of the invention. Other methods of fabrication are also feasible and perhaps equally viable. For clarity purposes, many of the reference numbers are eliminated from subsequent drawings so as to focus on the portion of interest of the semiconductor structure 300.

Figure 3B shows the semiconductor structure following the next sequence of processing. A thick insulation layer 320 is deposited overlying substrate 302 as well as field isolation regions 352, and active regions 350. Insulation layer 320 is an insulator material such as silicon oxide, silicon nitride, and silicon oxynitride. In one embodiment, insulation layer 320 is a doped insulator material such as borophosphosilicate glass (BPSG), a boron and phosphorous-doped silicon oxide. The insulation layer 320 is planarized, such as by chemical-mechanical planarization (CMP), in order to provide a uniform height.

Figure 3C shows the semiconductor structure following the next sequence of processing. A conductive layer 324 is formed abutting the insulation layer 320. The conductive layer 324 includes a conductive material. In one embodiment, the conductive layer 324 includes at least one conductive metal oxide. In another embodiment, the conductive metal oxide is selected from a group consisting of

ruthenium oxide and iridium oxide.

The conductive layer 324 may be formed by any method, such as collimated sputtering, chemical vapor deposition (CVD), or other deposition techniques. In this embodiment, the conductive layer 324 is patterned to form the bottom conductive layer, or bottom electrode, or bottom plate of a semiconductor structure of interest, such as a capacitor.

Figure 3D shows the semiconductor structure following the next sequence of processing. An insulation layer 326 is formed abutting the conductive layer 324. In one embodiment, the insulation layer 326 contains a dielectric material having a high dielectric constant. In another embodiment, the insulation layer 326 contains a dielectric material having a dielectric constant greater than about 7. In another embodiment, the insulation layer 326 contains a dielectric material having a dielectric constant greater than about 50. In yet another embodiment, the insulation layer 326 contains at least one metal oxide dielectric material. In a further embodiment, the insulation layer 326 contains ditantalum pentaoxide ( $\text{Ta}_2\text{O}_5$ ). The insulation layer 326 may be formed by any method, such as collimated sputtering, chemical vapor deposition, or other deposition techniques.

Figure 3E shows the semiconductor structure following the next sequence of processing. A conductive layer 328 is formed abutting the insulation layer 326. The conductive layer 328 includes a conductive material. In one embodiment, the conductive layer 328 includes at least one conductive metal oxide. In another embodiment, the conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide.

The conductive layer 328 may be formed by any method, such as collimated sputtering, chemical vapor deposition (CVD), or other deposition techniques. In this embodiment, the conductive layer 328 forms the top conductive layer, or top electrode, or top plate of a semiconductor structure of interest, such as a capacitor.

Figure 3F shows the semiconductor structure following the next sequence of processing. An inhibiting layer 330 is formed abutting the conductive layer 328. In one embodiment, the inhibiting layer comprises a material that is selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy. In another embodiment, the transition metal is selected from a group consisting of platinum, rhodium, and tungsten. In yet another embodiment, the transition metal alloy includes a platinum rhodium alloy. In a further embodiment, the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride. In another embodiment, the noble metal includes platinum, gold, titanium, and silver. In yet a further embodiment, the noble metal alloy includes graphite, chlorimet 3, and hastelloy C. In the embodiment in which the inhibiting layer 330 overlies the conductive layer 328, the inhibiting layer 330 may be formed by any suitable method, such as collimated sputtering, chemical vapor deposition (CVD), or physical vapor deposition. In the embodiment in which the inhibiting layer 330 is embedded in the conductive layer 328, the inhibiting layer 330 may be implanted using a shallow implantation technique or other suitable embedding techniques.

Figure 3G shows the semiconductor structure following the next sequence of processing. A mask 354 is formed abutting a portion of the inhibiting layer 330. The mask 354 is patterned to define future locations of the semiconductor structure of interest, such as a capacitor.

Figure 3H shows the semiconductor structure following the next sequence of processing. Portions of the inhibiting layer 330, conductive layer 338, insulation layer 336, and conductive layer 334 are exposed where the mask 354 does not cover. These exposed portions are selectively removed as well as the mask 354. Once these exposed portions are removed, semiconductor structures of interest, such as capacitors 336, are defined and remained abutting the insulation layer 320. These exposed portions may be removed by etching or by other suitable removal techniques known in the art. Removal

techniques are generally dependent upon the material of construction of the layer to be removed as well as the surrounding layers to be retained.

Figure 3I shows the semiconductor structure following the next sequence of processing. An insulation layer 322 is deposited abutting the capacitors 336 as well as insulation layer 320. Insulation layer 322 is an insulator material such as silicon oxide, silicon nitride, and silicon oxynitride. In one embodiment, insulation layer 322 is a doped insulator material such as borophosphosilicate glass (BPSG), a boron and phosphorous-doped silicon oxide. The insulation layer 322 is planarized, such as by chemical-mechanical planarization (CMP), in order to provide a uniform height.

Figure 3J shows the semiconductor structure following the next sequence of processing. Portions of the insulation layers 320 and 322 are selectively masked and patterned using any suitable photolithography techniques. Once masked and patterned, the insulation layers 320 and 322 are etched to define plugs or vias (hereinafter, holes). Once these portions are etched, holes 356<sub>0</sub> and 356<sub>1</sub> are defined to expose the inhibiting layers 330 of the capacitors 336 and the silicide contacts 308. Besides etching, these portions may be removed by other suitable removal techniques known in the art. Removal techniques are generally dependent upon the material of construction of the layer to be removed as well as the surrounding layers to be retained.

Figure 3K shows the semiconductor structure following the next sequence of processing. An insulation layer 358 is patterned and etched using any suitable photolithography techniques. The insulation layer 358 is defined to abut a portion of the insulation layer 322. Insulation layer 358 is an insulator material such as silicon oxide, silicon nitride, or silicon oxynitride. In one embodiment, insulation layer 358 is a doped insulator material such as borophosphosilicate glass (BPSG), a boron and phosphorous-doped silicon oxide. The insulation layer 358 is planarized, such as by chemical-mechanical planarization (CMP), in order to provide a uniform height.

Figure 3L shows the semiconductor structure following the next sequence of

processing. A first layer 360 of a metallization layer is formed to fill a portion of the holes 356<sub>0</sub> and 356<sub>1</sub>. The first layer 360 includes any conductive material that resists diffusion. Hence, the first layer 360 may be considered a diffusion barrier layer or a portion of a diffusion barrier layer of the metallization layer. In one embodiment, the first layer 360 includes a transition metal, such as titanium. In another embodiment, the first layer 360 includes a nitride compound, a carbide compound, a boride compound, a transition metal alloy, and a transition metal nitride compound alloy. In yet another embodiment, the nitride compound includes titanium nitride. In a further embodiment, the transition metal alloy includes titanium tungsten. In yet a further embodiment, the transition metal nitride compound alloy includes titanium nitride tungsten. In another embodiment, the first layer 360 may be selected from either a noble metal or a noble metal alloy. The noble metal includes platinum, gold, titanium, and silver. The noble metal alloy includes graphite, chlorimet 3, and hastelloy C. The first layer 360 may be formed by any method, such as collimated sputtering, chemical vapor deposition (CVD), or other deposition techniques.

Figure 3M shows the semiconductor structure following the next sequence of processing. A second layer 364 of a metallization layer is optionally formed through masking and patterning through a suitable photolithography technique. The second layer 364 is formed abutting the first layer 360 and the insulating layer 358. In one embodiment, the second layer 364 is a conductive layer that includes a transition metal, such as tungsten. The second layer 364 may be formed by any method, such as collimated sputtering, chemical vapor deposition (CVD), or other deposition techniques.

Figure 3N shows the semiconductor structure following the next sequence of processing. Another layer 368 of the metallization layer is formed abutting the second layer 364. The layer 368 includes any conductive material. In one embodiment, the layer 368 includes a transition metal, such as aluminum. The layer 368 may be formed by any method, such as collimated sputtering, chemical vapor deposition (CVD), or other

deposition techniques.

Figure 3O shows the semiconductor structure following the next sequence of processing. A digit line contact 341 is formed over the digit line contact regions 348. The formation of the digit line contact 341 and the completion of the semiconductor structure 300 do not limit the embodiments of the present invention and as such will not be discussed here in detail. Figure 3O shows a semiconductor structure complete with metallization layer 340 in contact with the source/drain regions 306 and the capacitors 336.

The inhibiting layer 330 acts to inhibit an open contact from occurring between the metallization layer 340 and the semiconductor structures of interest, such as capacitors 336. In one embodiment, the inhibiting layer 330 acts to inhibit formation of an undesired dielectric. In another embodiment, the inhibiting layer 330 acts to inhibit a diffusion that increases resistivity. In another embodiment, the inhibiting layer 330 acts to inhibit formation of an undesired oxidation compound so as to enhance an ohmic contact between the metallization layer 340 and the capacitors 336.

Figure 4 is a block diagram of a device according to one embodiment of the present invention. The memory device 400 includes an array of memory cells 402, address decoder 404, row access circuitry 406, column access circuitry 408, control circuitry 410, and input/output circuit 412. The memory device 400 can be coupled to an external microprocessor 414, or memory controller for memory accessing. The memory device 400 receives control signals from the processor 414, such as WE\*, RAS\* and CAS\* signals. The memory device 400 is used to store data which is accessed via I/O lines. It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device 400 has been simplified to help focus on the invention. At least one of the memory cells has an inhibiting layer in accordance with the aforementioned embodiments.

It will be understood that the above description of a DRAM (Dynamic Random



Access Memory) is intended to provide a general understanding of the memory and is not a complete description of all the elements and features of a DRAM. Further, the invention is equally applicable to any size and type of memory circuit and is not intended to be limited to the DRAM described above. Other alternative types of devices include SRAM (Static Random Access Memory) or Flash memories. Additionally, the DRAM could be a synchronous DRAM commonly referred to as SGRAM (Synchronous Graphics Random Access Memory), SDRAM (Synchronous Dynamic Random Access Memory), SDRAM II, and DDR SDRAM (Double Data Rate SDRAM), as well as Synchlink or Rambus DRAMs and other emerging memory technologies.

As recognized by those skilled in the art, memory devices of the type described herein are generally fabricated as an integrated circuit containing a variety of semiconductor devices. The integrated circuit is supported by a substrate. Integrated circuits are typically repeated multiple times on each substrate. The substrate is further processed to separate the integrated circuits into dies as is well known in the art.

Figure 5 is an elevation view of a semiconductor wafer according to one embodiment of the present invention. In one embodiment, a semiconductor die 510 is produced from a wafer 500. A die is an individual pattern, typically rectangular, on a substrate that contains circuitry, or integrated circuit devices, to perform a specific function. At least one of the integrated circuit devices includes a memory cell that has an inhibiting layer as discussed in the various embodiments heretofore in accordance with the invention. A semiconductor wafer will typically contain a repeated pattern of such dies containing the same functionality. Die 510 may contain circuitry for the inventive memory device, as discussed above. Die 510 may further contain additional circuitry to extend to such complex devices as a monolithic processor with multiple functionality. Die 510 is typically packaged in a protective casing (not shown) with leads extending therefrom (not shown) providing access to the circuitry of the die for

unilateral or bilateral communication and control.

Figure 6 is a block diagram of a circuit module according to one embodiment of the present invention. Two or more dies 610 may be combined, with or without protective casing, into a circuit module 600 to enhance or extend the functionality of an individual die 610. Circuit module 600 may be a combination of dies 610 representing a variety of functions, or a combination of dies 610 containing the same functionality. One or more dies 610 of circuit module 600 contain at least one inhibiting layer in accordance with the embodiments of the present invention.

Some examples of a circuit module include memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Circuit module 600 may be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others. Circuit module 600 will have a variety of leads 612 extending therefrom and coupled to the dies 610 providing unilateral or bilateral communication and control.

Figure 7 is a block diagram of a memory module according to one embodiment of the present invention. Memory module 700 contains multiple memory devices 710 contained on support 715, the number depending upon the desired bus width and the desire for parity. Memory module 700 accepts a command signal from an external controller (not shown) on a command link 720 and provides for data input and data output on data links 730. The command link 720 and data links 730 are connected to leads 740 extending from the support 715. Leads 740 are shown for conceptual purposes and are not limited to the positions as shown. At least one of the memory devices 710 includes a memory cell that includes an inhibiting layer as discussed in various embodiments in accordance with the invention.

Figure 8 is a block diagram of a system according to one embodiment of the present invention. Electronic system 800 contains one or more circuit modules 802. Electronic system 800 generally contains a user interface 804. User interface 804 provides a user of the electronic system 800 with some form of control or  
5 observation of the results of the electronic system 800. Some examples of user interface 804 include the keyboard, pointing device, monitor, or printer of a personal computer; the tuning dial, display, or speakers of a radio; the ignition switch, gauges, or gas pedal of an automobile; and the card reader, keypad, display, or currency dispenser of an automated teller machine. User interface 804 may further  
10 describe access ports provided to electronic system 800. Access ports are used to connect an electronic system to the more tangible user interface components previously exemplified. One or more of the circuit modules 802 may be a processor providing some form of manipulation, control, or direction of inputs from or outputs to user interface 804, or of other information either preprogrammed into, or  
15 otherwise provided to, electronic system 800. As will be apparent from the lists of examples previously given, electronic system 800 will often contain certain mechanical components (not shown) in addition to circuit modules 802 and user interface 804. It will be appreciated that the one or more circuit modules 802 in electronic system 800 can be replaced by a single integrated circuit. Furthermore,  
20 electronic system 800 may be a subcomponent of a larger electronic system. At least one of the circuit modules 802 includes a memory cell that includes an inhibiting layer as discussed in various embodiments in accordance with the invention.

Figure 9 is a block diagram of a system according to one embodiment of the present invention. Memory system 900 contains one or more memory modules 902  
25 and a memory controller 912. Each memory module 902 includes at least one memory device 910. Memory controller 912 provides and controls a bidirectional interface between memory system 900 and an external system bus 920. Memory

system 900 accepts a command signal from the external bus 920 and relays it to the one or more memory modules 902 on a command link 930. Memory system 900 provides for data input and data output between the one or more memory modules 902 and external system bus 920 on data links 940. At least one of the memory devices 910 includes a memory cell that includes an inhibiting layer as discussed in various embodiments in accordance with the invention.

Figure 10 is a block diagram of a system according to one embodiment of the present invention. Computer system 1000 contains a processor 1010 and a memory system 1002 housed in a computer unit 1005. Computer system 1000 is but one example of an electronic system containing another electronic system, e.g., memory system 1002, as a subcomponent. The memory system 1002 may include a memory cell that includes an inhibiting layer as discussed in various embodiments of the present invention. Computer system 1000 optionally contains user interface components. These user interface components include a keyboard 1020, a pointing device 1030, a monitor 1040, a printer 1050, and a bulk storage device 1060. It will be appreciated that other components are often associated with computer system 1000 such as modems, device driver cards, additional storage devices, etc. It will further be appreciated that the processor 1010 and memory system 1002 of computer system 1000 can be incorporated on a single integrated circuit. Such single-package processing units reduce the communication time between the processor and the memory circuit.

### Conclusion

Systems, devices, structures, and methods have been described to address situations where a metallization layer acts with one of the conductive layers of a capacitor such that an opened contact exists between the metallization layer and the capacitor. Capacitors that use the inhibiting layer as described heretofore benefit from the dual ability of having an increase in storage capability yet a decrease in space requirement. As described heretofore, the inhibiting layer inhibits diffusion between two solids at a predetermined temperature. The inhibition of such diffusion allows a capacitor to maintain good ohmic contact with the metallization layer. However, the inhibiting layer may also inhibit diffusion of molecules that may come from other parts of the semiconductor structure, such as the dielectric of the capacitor. While the various embodiments described heretofore have discussed the inhibition of diffusion of oxygen molecules, the structures and methods described can be used to inhibit diffusion of other chemical species through an appropriate choice of materials for the inhibiting layer.

Although the specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention includes any other applications in which the above structures and fabrication methods are used. Accordingly, the scope of the invention should only be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.